GEORGIA TECH GT-VFPU
VLSI DESIGN VERIFICATION DOCUMENT

VLSI DEVELOPMENT REPORT

REPORT NO. VDR-0142-90-001

MAY 15, 1990

GUIDANCE, NAVIGATION AND CONTROL
DIGITAL EMULATION TECHNOLOGY LABORATORY

Contract No. DASG60-89-C-0142

Sponsored By

The United States Army Strategic Defense Command

COMPUTER ENGINEERING RESEARCH LABORATORY
Georgia Institute of Technology
Atlanta, Georgia 30332 - 0540

Contract Data Requirements List Item A006

Period Covered: Not Applicable

Type Report: As Required

DISCLAIMER

DISTRIBUTION CONTROL

GEORGIA TECH GT-VFPU
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May 15, 1990

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GEORGIA TECH GT-VFPU

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1.0 INTRODUCTION

There are eleven (11) Georgia Tech VLSI designs (see Table 1) in the AHAT Program. Each of these designs has been produced by Georgia Tech using the Genesil Silicon Compiler. Each design has passed the design verification process at Silicon Compiler Systems/Mentor Graphics and each has been fabricated in a bulk CMOS process (fabrication of certain chips was not complete when this document was released). Each of the Georgia Tech designs listed in Table 1 is being delivered to USASDC and to the Harris Corporation for conversion and fabrication in a rad-hard process. The program under which this work is done is AHAT (Advanced Hardened Avionics Technology). This document includes design information for the Georgia Tech floating point unit, GT-VFPU.

TABLE 1. GEORGIA TECH CHIP SET FOR AHAT

DESIGN	DV PASSED	TAPE DELIV.	FABRICATED	TESTED
GT-VFPU				
GT-VNUC				
GT-VTF				
GT-VTHR				
GT-VCLS				
GT-VCTR				
GT-VIAG				
GT-VDAG				
GT-VSNI				
GT-VSM8				
GT-VSF				

1. Scheduled March 31, 1991
2. Scheduled December 31, 1990

Table of Contents

APPENDIX A
DESIGN VERIFICATION CHECKLIST

1. DV CONTROL NUMBER : ______________ (Assigned by SCS)

2. CUSTOMER INFORMATION

Customer Name: ______________ Chip Name: ______________

Project Manager: ______________ Phone: ______________

Design Engineer: Sam Russ Phone: (404) 894-3374

______________ Phone: ______________

Test Engineer : ______________ Phone: ______________

3. SCS CONTACT: Girish Kumar

4. REGRESSION

4.1 GENESIL Version: v7.0
4.2 Name of Session Log from recompile: REBUILD.CMD
4.3 Include DV_regression.001?: yes (simulation and timing)
4.4 Size of database: ______________ Density: 6250___ 1600___ TK50 X

5. FUNCTIONAL INFORMATION (check when included)

5.1 Key Parameters : ______________
5.2 DV_pin_description : ______________
5.3 Block Diagram : ______________
5.4 Functional Description : ______________
5.4 Timing Diagrams at Pins : ______________
5.6 Annotated Views : ______________ Annotated Schematics: ______________

6. PHYSICAL INFORMATION

6.1 Fabline : NSC CN12A

6.2 Plots: (check when included or indicate filename)
Chip Route (D size): x Bonding Diagram (B size) : ______________
Route Filename: route_d_1.031 Bonding Filename: bond_b_1.031

6.3 Die Size: (in mils) Reported Die Size: 378.~~95~~ 47 X 363.12
Maximum Acceptable Die Size: 392 X 392
Minimum Acceptable Die Size: 232 X 232

6.4 GENESIL Package Name : CPGA144f Spec included?: no
Cavity/Well Size : 472 mils by 472 mils

6.5 External Block: none

7. ELECTRICAL INFORMATION

7.1 Chip Frequency
Specified in netlist: 10 MHz Target frequency: 6.7 MHz (1/150 ns)

7.2 Power Dissipation: GENESIL= 5.1 W at 10 MHz Spec= 1.5 W at 10 MHz

7.3 Operating Voltage: from 4.5 Volts to 5.5 Volts

8. SIMULATION

8.1 Number of Clocking Regimes : one

	Clock Pad Name	DIV/NO DIV	Ext Clock Name	Int PHASE A/PHASE B Name
1.	clock pad	NO DIV	proc_clk	PHASE_A/PHASE_B
2.				
3.				
4.				
5.				

8.2 Simulation Setup Files:

Name: ______ Listings attached: ______

Description: ______

Affected Tests: ______

Name: ______ Listings attached: ______

Description: ______

Affected Tests: ______

Name: ______ Listings attached: ______

Description: ______

Affected Tests: ______

8.3 Test Vector Set:

NOTE: Test vectors written one phase per vector have a maximum test frequency on the IMS Tester of 10 MHz.
Test vectors written one cycle per vector have a maximum test frequency on the IMS Tester of 20 MHz.

1. Name: monolithic.089/083 No of vectors: 901
Description: Functional test of all opcodes, as well as some manuf. testing of adder, normalizer, multiplier, and fixed pt modules.

Portions of Chip Tested: All

Run with GFL model? x Use for switch level simulation? ~~Y~~ N
Run with GSL model? x Use for tester? ~~Y~~ N

2. Name: test2op.083 No of vectors: 7622
Description: tests 2-operand opcodes

Portions of Chip Tested: all

Run with GFL model? x Use for switch level simulation? ~~Y~~ N
Run with GSL model? x Use for tester? ~~Y~~ N

3. Name: testRop.083 No of vectors: 2998
Description: tests "R-operand" opcodes

Portions of Chip Tested: all

Run with GFL model? x Use for switch level simulation? ~~Y~~ N
Run with GSL model? x Use for tester? ~~Y~~ N

4. Name: testSop.083 No of vectors: 1910
Description: test S-operand opcodes

Portions of Chip Tested: all

Run with GFL model? X Use for switch level simulation? Y N
Run with GSL model? X Use for tester? Y N

5. Name: add_atg.083 No of vectors: 1542
Description: additional tests of adder

Portions of Chip Tested: adder, normalizer

Run with GFL model? X Use for switch level simulation? Y N
Run with GSL model? X Use for tester? Y N

6. Name: testshop.083 No of vectors: 774
Description: Tests shift and rotate opcodes
Description:

Portions of Chip Tested: "barrel" module

Run with GFL model? Use for switch level simulation? Y N
Run with GSL model? Use for tester? Y N

7. Name: ~~add_vecs.083~~ No of vectors: ~~1578~~
Description: ~~AIG output of adder testing~~

Portions of Chip Tested: ~~Adder~~

Run with GFL model? X Use for switch level simulation? Y N
Run with GSL model? X Use for tester? Y N

8. Name: ftest.083 No of vectors: 46
Description:
Tests F bus enable circuitry, "Flush" and "Freeze" logic

Portions of Chip Tested: F_bus_enable, F_pad's, Flush, Freeze (output module)

Run with GFL model? ___ Use for switch level simulation? Y N
Run with GSL model? ___ Use for tester? Y N

9. TIMING ANALYSIS

9.1 Environment

```
Temperature Coefficient:   35         Degrees C / Watt (theta_JA)
Operating Temp      : from   0    C (min)   to  75    C (max)
Operating Voltage   : from  4.5   V (min)   to  5.5   V (max)

room junction temp = 25 + (theta_JA * Power)  =  133.5   degrees C
maximum junction temp =
    maximum ambient temp + (theta_JA * Power) =  183.5   degrees C
```

9.2 Include the following reports:

```
   (required)                 (required)                 (optional)
 guaranteed model           guaranteed model           target model
    5.0V                    min operating V            min operating V
 room junc temp(100°C)      max junction temp(150°C)   max junction temp
 ----------------           ----------------           ----------------
         Cycle: X                   Cycle: X                   Cycle: ___
    Setup/Hold: X              Setup/Hold: X              Setup/Hold: ___
  Output Delay: X            Output Delay: X            Output Delay: ___
    Path Delay: X              Path Delay: X              Path Delay: ___
```

9.3 Setup Files:

Name: ignore_setup Listings attached: ________
Temperature: 100°C Voltage: 5.0 V

Description : Used for cycle time calculations only. Sets setup time for ALU opcode and operand select (R/S_eq_f_1/2) to -999, since these are actually SB(t) signals from other chips.

Name: include_setup Listings attached: ________
Temperature: 100°C Voltage: 5.0 V

Description : Used for all other reports at 100°C.

Name: ignore_high Listings attached: ________
Temperature: 150°C Voltage: 4.5V

Description : Used for cycle time calculations at 150°C.

Name: include_high Listings attached: ________
Temperature: 150°C Voltage: 4.5 V

Description : Used for all other reports at 150°C.

9.4 Critical Boundary Conditions:

List critical paths here or annotate the timing report.
Attach additional pages if needed.

Clock Name: proc_clk

	report	limit	report	limit
1. Phase 1 High	16.9	75.0		
2. Phase 2 High	6.3	75.0		
3. Symmetric Cycle	154.6	150.0		
4. Minimum Cycle	154.6	150.0		

Outputs

	Signal Name	load (pF)	delay	limit
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				

Inputs

	Signal Name	setup report/limit	hold report/limit
1.		/	/
2.		/	/
3.		/	/
4.		/	/
5.		/	/
6.		/	/
7.		/	/
8.		/	/
9.		/	/
10.		/	/

9.5 Hold Time Violations: none (At 2 nsec.)

11. TAPEOUT AND TESTING SPECIFICATION

Prototype Brokerage Service Purchased? _______yes _______no
If yes: PO #________________

12. CUSTOMER CHECKLIST COMMENTS

Pre-Verification Comments

SCS will report back on the fault coverage of our test vector set.
We reserve the right to submit additional vectors, at no extra cost,
if we decide that the fault coverage is not sufficiently high.

13. CUSTOMER CHECKLIST APPROVAL

The undersigned understands that if any design changes are initiated by the Customer subsequent to this sign-off, the Customer is liable for any charges imposed by Silicon Compiler Systems as agreed to in either the Design Verification Terms & Conditions or the Prototype Brokerage Services Terms & Conditions. In addition, such changes require the DV process to be started from the beginning, which results in extended DV schedules.

Customer Approval : ________________________ Date ____/___/____

Title : ________________________

14. SCS CHECKLIST APPROVAL

Pre-Verification Comments

SCS Approval : ________________________ Date ____/___/___

Title : ________________________

DESIGN VERIFICATION NOTES FOR fpu

1. Design enhancements

For your information, the following changes were made.

Normalizer - Replaced PLA's with Genesil's Datapath Static Barrel Shifter
Barrel - Added this module to perform barrel shifts and rotates. It is logic compiled.
Fixed_pt - Changed to handle barrel shifter outputs
Input - Added "freeze" option
Output - Added "freeze" and "flush" options
Pads - Added a "Freeze" and a "Flush" pad. Both have been bonded successfully.

All of the changes have been reflected in the documentation, and the chip database is fully compiled with no errors.

2. Test vectors

Filename	Size	Traceobj version	Size
monolithic	869	mon_trace	1739
add_atg	1542	add_trace	3085
test2op	7622	test2_trace	15425
testRop	2454	testR_trace	4909
testSop	1366	testS_trace	2733
testshop	774	testsh_trace	1549
ftest	46	ftest_trace	93

The "regular" files are one vector per cycle, and the traceobj files are one vector per phase. Of course, these are the "latest" vectors and should all run properly under GFL. I will try to run GSL here and let you know if there are any problems.

3. Power consumption

The chip consumes about 3.1 Watts. However, the key parameters listing no longer produces figures for power consumption. The key parameters listing is found under /fpu/keyparm.106 and the tnet power report is found under /fpu/Power.106. They are also enclosed as hardcopy. The vast majority of the remaining DC power is due to high-speed static adders. They were not changed to low power for three reasons. First, they are on various critical timing paths. Second, in the case of the "shift_mant" module, add/subtract capability was needed, and this is not possible with low-power static adders. Third, the 3.1 Watt figure is acceptable.

```
UTILITY;
KEY_PARAMETERS

 Key Parameters for Chip  ~sfpu/sfpu/fpu
 ----------------------------------------

 ROUTE_VERSION = 87.20
 HEIGHT = 367.5 MILS
    ( = 9334.50 u )
 WIDTH = 373.5 MILS
    ( = 9486.90 u )
 ROUTED = 1 (0=NO,1=YES)
 TOTAL_WIRE_LENGTH = 1168070 MILS
    ( = 29668978. u )
 CORE_AREA = 109333.2 SQUARE_MILS
    ( = 70537410.6 u2 )
 PADRING_AREA = 27936.8 SQUARE_MILS
    ( = 18023706. u2 )
 PAD_AREA = 24909.8 SQUARE_MILS
    ( = 16070807. u2 )
 ROUTE_AREA = 62919.0 SQUARE_MILS
    ( = 40592822. u2 )
 PERCENT_ROUTING_OF_CORE = 57 %
 PERCENT_ROUTING_OF_CHIP = 45 %
 PERCENT_CORE_OF_CHIP = 79 %
 PERCENT_PADRING_OF_CHIP = 20 %
 PERCENT_PAD_OF_PADRING = 89 %

 NETLIST_VERSION = 1.0
 NETLIST_EXISTS = 1 (0=NO,1=YES)

 PHASE_A_TIME = 28.7 NANOSECONDS
 PHASE_B_TIME = 14.1 NANOSECONDS
 SYMMETRIC_TIME = 116.6 NANOSECONDS


 ROUTE_ESTIMATE_LVL = 0
 FLAT_ROUTE = 1 (0=NO,1=YES)
 TECHNOLOGY_NAME = CMOS-1
 PACKAGE_SPECIFIED = 1 (0=NO,1=YES)
 PACKAGE_NAME = CPGA144f
 FABLINE_NAME = NSC_CN12A
 COMPILER_TYPE = GCX

 FLOORPLAN_VERSION = 7.0
 BOND_PAD_CNT = 138
 HEIGHT_ESTIMATE = 381.85 MILS
    ( = 9698.990 u )
 WIDTH_ESTIMATE = 398.19 MILS
    ( = 10114.02 u )
 FUSED = 1 (0=NO,1=YES)
 FUSION_REQUIRED = 1 (0=NO,1=YES)
 PINOUT = 1 (0=NO,1=YES)
 PINOUT_REQUIRED = 1 (0=NO,1=YES)
 PLACED = 1 (0=NO,1=YES)
 PLACEMENT_REQUIRED = 1 (0=NO,1=YES)
```

```
DOWN_BONDS_ALLOWED = 1 (0=NO,1=YES)
PKG_PIN_COUNT = 144
PKG_WELL_HEIGHT = 472.00 MILS
   ( = 11988.80 u )
PKG_WELL_WIDTH = 472.00 MILS
   ( = 11988.80 u )
AREA = 137261.3 SQUARE_MILS
   ( = 88555499.9 u2 )
OBJECT_TYPE = Chip
PHYSICAL_IMPLEMENTATIONS_EXIST = 0 (0=NO,1=YES)
CHECKPOINTS_EXIST = 1 (0=NO,1=YES)
CAN_SET_FABLINE = 1 (0=NO,1=YES)

Key Parameter Listing Complete
```

```
START Genesil job ~sfpu/sfpu/18_Aug_1 on calsc2 Thu Aug 18 16:40:37 1988
```



```
ONTINUE
el do fpu ba
un TNET
DISP_POWER
OWER
 Clock Proc_clk [clock=-9999]
 Reading Routing Data . . .
 INFO: longest net delay: 26.1ns
    Nets with delay longer than 10.0ns are recorded in ancilLary file LONG_NET
  STD
 INFO: Nets loading, driving information can be found in ancillary file TA_NET
  STD
 Back-annotating route capacitance for block power calculation. . .
  Power for block ringpower: 0.00mW(DC) 0.00mW(AC)
  Power for block ringground: 0.00mW(DC) 0.00mW(AC)
  Power for block reset_pad: 0.00mW(DC) 0.35mW(AC)
  Power for block output/resultsel: 0.00mW(DC) 0.98mW(AC)
  Power for block output/result_handler: 4.46mW(DC) 31.02mW(AC)
  Power for block output/outputmux: 65.67mW(DC) 2.51mW(AC)
  Power for block output/outmux2: 58.92mW(DC) 2.63mW(AC)
  Power for block output/mantmux: 0.00mW(DC) 9.08mW(AC)
  Power for block output/logic: 0.00mW(DC) 1.04mW(AC)
  Power for block output/flagsel: 0.00mW(DC) 1.34mW(AC)
  Power for block output/flagreg: 0.00mW(DC) 1.42mW(AC)
  Power for block output/f_disable: 0.00mW(DC) 1.01mW(AC)
  Power for block output/expmux: 0.00mW(DC) 3.16mW(AC)
  Power for block opcode_logic/oplatch: 0.00mW(DC) 1.71mW(AC)
  Power for block opcode_logic/notop: 0.00mW(DC) 0.52mW(AC)
  Power for block opcode_logic/fplatch: 0.00mW(DC) 2.88mW(AC)
  Power for block opcode_logic/fpcon2: 0.00mW(DC) 0.25mW(AC)
  Power for block opcode_logic/fpcon1: 0.00mW(DC) 0.39mW(AC)
 W: Node normalizer/left_shift/postnorm[24] is not routed
```

```
W: Node normalizer/left_shift/postnorm[0] is not routed
 Power for block normalizer/left_shift: 0.00mW(DC) 9.60mW(AC)
 Power for block normalizer/flags: 0.00mW(DC) 0.16mW(AC)
 Power for block normalizer/exponent: 72.86mW(DC) 4.14mW(AC)
 Power for block normalizer/encoderc: 0.00mW(DC) 0.60mW(AC)
 Power for block normalizer/encoderb: 0.00mW(DC) 0.62mW(AC)
 Power for block normalizer/encodera: 0.00mW(DC) 0.59mW(AC)
 Power for block normalizer/cascade: 0.00mW(DC) 0.74mW(AC)
 Power for block mult/sign_ovfl: 0.00mW(DC) 0.57mW(AC)
W: Node mult/normalize/result[32] is not routed
 Power for block mult/normalize: 0.00mW(DC) 4.22mW(AC)
 Power for block mult/multac: 0.00mW(DC) 33.07mW(AC)
 Power for block mult/multab: 0.00mW(DC) 33.06mW(AC)
 Power for block mult/fxd_res: 8.92mW(DC) 4.05mW(AC)
 Power for block mult/add_out_lo: 113.22mW(DC) 5.99mW(AC)
 Power for block mult/add_hi: 425.06mW(DC) 24.06mW(AC)
 Power for block mult/add_exp: 233.00mW(DC) 6.72mW(AC)
 Power for block mult/add_ac_hi: 212.53mW(DC) 12.31mW(AC)
 Power for block input/op_sel_logic: 0.00mW(DC) 0.34mW(AC)
 Power for block input/latch: 0.00mW(DC) 1.93mW(AC)
 Power for block input/inputmux: 303.68mW(DC) 1.60mW(AC)
 Power for block input/b_low: 0.00mW(DC) 12.01mW(AC)
 Power for block input/b_input: 8.92mW(DC) 7.71mW(AC)
 Power for block input/b_high: 0.00mW(DC) 3.65mW(AC)
 Power for block input/a_low: 0.00mW(DC) 12.62mW(AC)
 Power for block input/a_input: 4.46mW(DC) 7.88mW(AC)
 Power for block input/a_high: 0.00mW(DC) 3.04mW(AC)
 Power for block fixed_pt/synch: 0.00mW(DC) 0.73mW(AC)
W: Node fixed_pt/flag_zero/sro_s is not routed
W: Node fixed_pt/flag_zero/sro_r is not routed
W: Node fixed_pt/flag_zero/slo_s is not routed
W: Node fixed_pt/flag_zero/slo_r is not routed
 Power for block fixed_pt/fixed_pt_alu: 288.69mW(DC) 29.19mW(AC)
 Power for block cornerpwr: 0.00mW(DC) 0.00mW(AC)
 Power for block cornergnd: 0.00mW(DC) 0.00mW(AC)
 Power for block corepower: 0.00mW(DC) 0.00mW(AC)
 Power for block coreground: 0.00mW(DC) 0.00mW(AC)
 Power for block clock_pad: 0.00mW(DC) 23.25mW(AC)
 Power for block barrel: 0.00mW(DC) 26.57mW(AC)
 Power for block adder/subtract: 223.94mW(DC) 13.63mW(AC)
 Power for block adder/sign_logic: 0.00mW(DC) 0.94mW(AC)
W: Node adder/shift_mant/addout[1] is not routed
W: Node adder/shift_mant/addout[0] is not routed
W: Node adder/shift_mant/postshift[19] is not routed
W: Node adder/shift_mant/postshift[18] is not routed
W: Node adder/shift_mant/postshift[17] is not routed
W: Node adder/shift_mant/addout[19] is not routed
W: Node adder/shift_mant/postshift[16] is not routed
W: Node adder/shift_mant/addout[18] is not routed
W: Node adder/shift_mant/addout[17] is not routed
W: Node adder/shift_mant/postshift[15] is not routed
W: Node adder/shift_mant/addout[16] is not routed
W: Node adder/shift_mant/postshift[9] is not routed
W: Node adder/shift_mant/postshift[14] is not routed
W: Node adder/shift_mant/addout[25] is not routed
W: Node adder/shift_mant/addout[15] is not routed
```

```
W: Node adder/shift_mant/postshift[8] is not routed
W: Node adder/shift_mant/postshift[13] is not routed
W: Node adder/shift_mant/addout[24] is not routed
W: Node adder/shift_mant/addout[14] is not routed
W: Node adder/shift_mant/postshift[7] is not routed
W: Node adder/shift_mant/addout[23] is not routed
W: Node adder/shift_mant/addout[13] is not routed
W: Node adder/shift_mant/postshift[12] is not routed
W: Node adder/shift_mant/postshift[6] is not routed
W: Node adder/shift_mant/addout[22] is not routed
W: Node adder/shift_mant/addout[12] is not routed
W: Node adder/shift_mant/postshift[11] is not routed
W: Node adder/shift_mant/addout[21] is not routed
W: Node adder/shift_mant/addout[11] is not routed
W: Node adder/shift_mant/postshift[5] is not routed
W: Node adder/shift_mant/postshift[10] is not routed
W: Node adder/shift_mant/addout[20] is not routed
W: Node adder/shift_mant/addout[10] is not routed
W: Node adder/shift_mant/postshift[4] is not routed
W: Node adder/shift_mant/postshift[3] is not routed
W: Node adder/shift_mant/postshift[2] is not routed
W: Node adder/shift_mant/postshift[26] is not routed
W: Node adder/shift_mant/postshift[1] is not routed
W: Node adder/shift_mant/postshift[25] is not routed
W: Node adder/shift_mant/postshift[24] is not routed
W: Node adder/shift_mant/postshift[23] is not routed
W: Node adder/shift_mant/postshift[22] is not routed
W: Node adder/shift_mant/postshift[21] is not routed
W: Node adder/shift_mant/sum_mant[26] is not routed
W: Node adder/shift_mant/postshift[20] is not routed
W: Node adder/shift_mant/addout[9] is not routed
W: Node adder/shift_mant/addout[8] is not routed
W: Node adder/shift_mant/addout[7] is not routed
W: Node adder/shift_mant/sum_mant[0] is not routed
W: Node adder/shift_mant/addout[6] is not routed
W: Node adder/shift_mant/addout[5] is not routed
W: Node adder/shift_mant/addout[4] is not routed
W: Node adder/shift_mant/addout[3] is not routed
W: Node adder/shift_mant/addout[2] is not routed
 Power for block adder/shift_mant: 548.99mW(DC) 44.47mW(AC)
 Power for block adder/shift_logic: 0.00mW(DC) 0.52mW(AC)
 Power for block adder/logic: 0.00mW(DC) 0.10mW(AC)
 Power for block Zero_pad: 0.00mW(DC) 4.21mW(AC)
 Power for block Test_pad: 0.00mW(DC) 0.19mW(AC)
 Power for block S_pad[9]: 0.00mW(DC) 0.16mW(AC)
 Power for block S_pad[8]: 0.00mW(DC) 0.16mW(AC)
 Power for block S_pad[7]: 0.00mW(DC) 0.15mW(AC)
 Power for block S_pad[6]: 0.00mW(DC) 0.15mW(AC)
 Power for block S_pad[5]: 0.00mW(DC) 0.15mW(AC)
 Power for block S_pad[4]: 0.00mW(DC) 0.15mW(AC)
 Power for block S_pad[3]: 0.00mW(DC) 0.15mW(AC)
 Power for block S_pad[31]: 0.00mW(DC) 0.28mW(AC)
 Power for block S_pad[30]: 0.00mW(DC) 0.28mW(AC)
 Power for block S_pad[2]: 0.00mW(DC) 0.16mW(AC)
 Power for block S_pad[29]: 0.00mW(DC) 0.27mW(AC)
 Power for block S_pad[28]: 0.00mW(DC) 0.27mW(AC)
```

```
Power for block S_pad[27]: 0.00mW(DC) 0.26mW(AC)
Power for block S_pad[26]: 0.00mW(DC) 0.25mW(AC)
Power for block S_pad[25]: 0.00mW(DC) 0.25mW(AC)
Power for block S_pad[24]: 0.00mW(DC) 0.24mW(AC)
Power for block S_pad[23]: 0.00mW(DC) 0.24mW(AC)
Power for block S_pad[22]: 0.00mW(DC) 0.23mW(AC)
Power for block S_pad[21]: 0.00mW(DC) 0.23mW(AC)
Power for block S_pad[20]: 0.00mW(DC) 0.22mW(AC)
Power for block S_pad[1]: 0.00mW(DC) 0.18mW(AC)
Power for block S_pad[19]: 0.00mW(DC) 0.21mW(AC)
Power for block S_pad[18]: 0.00mW(DC) 0.21mW(AC)
Power for block S_pad[17]: 0.00mW(DC) 0.20mW(AC)
Power for block S_pad[16]: 0.00mW(DC) 0.20mW(AC)
Power for block S_pad[15]: 0.00mW(DC) 0.20mW(AC)
Power for block S_pad[14]: 0.00mW(DC) 0.19mW(AC)
Power for block S_pad[13]: 0.00mW(DC) 0.18mW(AC)
Power for block S_pad[12]: 0.00mW(DC) 0.18mW(AC)
Power for block S_pad[11]: 0.00mW(DC) 0.17mW(AC)
Power for block S_pad[10]: 0.00mW(DC) 0.17mW(AC)
Power for block S_pad[0]: 0.00mW(DC) 0.19mW(AC)
Power for block Run_pad: 0.00mW(DC) 0.36mW(AC)
Power for block R_pad[9]: 0.00mW(DC) 0.21mW(AC)
Power for block R_pad[8]: 0.00mW(DC) 0.22mW(AC)
Power for block R_pad[7]: 0.00mW(DC) 0.22mW(AC)
Power for block R_pad[6]: 0.00mW(DC) 0.22mW(AC)
Power for block R_pad[5]: 0.00mW(DC) 0.23mW(AC)
Power for block R_pad[4]: 0.00mW(DC) 0.23mW(AC)
Power for block R_pad[3]: 0.00mW(DC) 0.24mW(AC)
Power for block R_pad[31]: 0.00mW(DC) 0.19mW(AC)
Power for block R_pad[30]: 0.00mW(DC) 0.19mW(AC)
Power for block R_pad[2]: 0.00mW(DC) 0.24mW(AC)
Power for block R_pad[29]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[28]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[27]: 0.00mW(DC) 0.17mW(AC)
Power for block R_pad[26]: 0.00mW(DC) 0.17mW(AC)
Power for block R_pad[25]: 0.00mW(DC) 0.16mW(AC)
Power for block R_pad[24]: 0.00mW(DC) 0.16mW(AC)
Power for block R_pad[23]: 0.00mW(DC) 0.15mW(AC)
Power for block R_pad[22]: 0.00mW(DC) 0.15mW(AC)
Power for block R_pad[21]: 0.00mW(DC) 0.15mW(AC)
Power for block R_pad[20]: 0.00mW(DC) 0.16mW(AC)
Power for block R_pad[1]: 0.00mW(DC) 0.24mW(AC)
Power for block R_pad[19]: 0.00mW(DC) 0.16mW(AC)
Power for block R_pad[18]: 0.00mW(DC) 0.17mW(AC)
Power for block R_pad[17]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[16]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[15]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[14]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[13]: 0.00mW(DC) 0.18mW(AC)
Power for block R_pad[12]: 0.00mW(DC) 0.19mW(AC)
Power for block R_pad[11]: 0.00mW(DC) 0.20mW(AC)
Power for block R_pad[10]: 0.00mW(DC) 0.21mW(AC)
Power for block R_pad[0]: 0.00mW(DC) 0.25mW(AC)
Power for block Ovfl_pad: 0.00mW(DC) 4.21mW(AC)
Power for block Op_sel_pad[3]: 0.00mW(DC) 0.26mW(AC)
Power for block Op_sel_pad[2]: 0.00mW(DC) 0.24mW(AC)
```

```
  Power for block Op_sel_pad[1]: 0.00mW(DC) 0.25mW(AC)
  Power for block Op_sel_pad[0]: 0.00mW(DC) 0.23mW(AC)
  Power for block Freeze_pad: 0.00mW(DC) 1.12mW(AC)
  Power for block Flush_pad: 0.00mW(DC) 0.35mW(AC)
  Power for block F_enable_pad[1]: 0.00mW(DC) 0.33mW(AC)
  Power for block F_enable_pad[0]: 0.00mW(DC) 0.33mW(AC)
  Power for block F8_pad[3]: 0.00mW(DC) 3.23mW(AC)
  Power for block F8_pad[2]: 0.00mW(DC) 3.23mW(AC)
  Power for block F8_pad[1]: 0.00mW(DC) 3.23mW(AC)
  Power for block F8_pad[0]: 0.00mW(DC) 3.23mW(AC)
  Power for block F7_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F7_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F7_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F7_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F6_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F6_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F6_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F6_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F5_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F5_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F5_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F5_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F4_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F4_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F4_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F4_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F3_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F3_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F3_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F3_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F2_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F2_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F2_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F2_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block F1_pad[3]: 0.00mW(DC) 3.20mW(AC)
  Power for block F1_pad[2]: 0.00mW(DC) 3.20mW(AC)
  Power for block F1_pad[1]: 0.00mW(DC) 3.20mW(AC)
  Power for block F1_pad[0]: 0.00mW(DC) 3.20mW(AC)
  Power for block Carry_pad: 0.00mW(DC) 4.21mW(AC)
  Power for block Alu_op_pad[4]: 0.00mW(DC) 0.50mW(AC)
  Power for block Alu_op_pad[3]: 0.00mW(DC) 0.49mW(AC)
  Power for block Alu_op_pad[2]: 0.00mW(DC) 0.45mW(AC)
  Power for block Alu_op_pad[1]: 0.00mW(DC) 0.52mW(AC)
  Power for block Alu_op_pad[0]: 0.00mW(DC) 0.51mW(AC)
 Total power consumption (5.5V, 0 DegC 50pf/out pad):
        DC:          2573.32mW [2573.32(core)+0.00(ring)]
        AC@10MHz:    524.92mW [386.52(core)+138.40(ring)]
BACK
EXIT_GENESIL
ONFIRM
EEP_LOG
 End of GENESIL session '18_Aug_1'
 +++++++++++++++++
```

NORTH

PAD NAME	PIN NUMBER	SIGNAL NAME	IN/OUT
cornergnd[1]	1	VSS	
F2_pad[0]	2	F[4]	OUT
F2_pad[1]	3	F[5]	OUT
F2_pad[2]	4	F[6]	OUT
F2_pad[3]	5	F[7]	OUT
ringpower[1]	6	VDD	
F3_pad[0]	7	F[8]	OUT
F3_pad[1]	8	F[9]	OUT
F3_pad[2]	9	F[10]	OUT
F3_pad[3]	10	F[11]	OUT
ringground[1]	11	VSS	
ringpower[2]	13	VDD	
F4_pad[0]	14	F[12]	OUT
F4_pad[1]	15	F[13]	OUT
F4_pad[2]	16	F[14]	OUT
F4_pad[3]	17	F[15]	OUT
ringground[2]	18	VSS	
ringpower[3]	19	VDD	
F5_pad[0]	20	F[16]	OUT
F5_pad[1]	21	F[17]	OUT
F5_pad[2]	22	F[18]	OUT
F5_pad[3]	23	F[19]	OUT
ringground[3]	24	VSS	
ringpower[4]	25	VDD	
F6_pad[0]	26	F[20]	OUT
F6_pad[1]	27	F[21]	OUT
F6_pad[2]	28	F[22]	OUT
F6_pad[3]	29	F[23]	OUT
ringground[4]	30	VDD	
F7_pad[0]	31	F[24]	OUT
F7_pad[1]	32	F[25]	OUT
F7_pad[2]	33	F[26]	OUT
F7_pad[3]	34	F[27]	OUT

EAST

PAD NAME	PIN NUMBER	SIGNAL NAME	IN/OUT
cornerpwr[0]	36	VDD	
ringpower[5]	37	VDD	
F8_pad[0]	38	F[28]	OUT
F8_pad[1]	39	F[29]	OUT
F8_pad[2]	40	F[30]	OUT
F8_pad[3]	41	F[31]	OUT
ringground[5]	42	VSS	
Alu_op_pad[4]	43	ALU_opcode[4]	IN
Alu_op_pad[3]	44	ALU_opcode[3]	IN
Alu_op_pad[2]	45	ALU_opcode[2]	IN
Alu_op_pad[1]	46	ALU_opcode[1]	IN
Alu_op_pad[0]	47	ALU_opcode[0]	IN
corepower[1]	48	VDD	
S_pad[31]	49	S[31]	IN
S_pad[30]	50	S[30]	IN
S_pad[29]	51	S[29]	IN
S_pad[28]	52	S[28]	IN
Test_pad	53	Test	IN
S_pad[27]	54	S[27]	IN
S_pad[26]	55	S[26]	IN
S_pad[25]	56	S[25]	IN
S_pad[24]	57	S[24]	IN
S_pad[23]	58	S[23]	IN
S_pad[22]	59	S[22]	IN
S_pad[21]	60	S[21]	IN
corepower[0]	61	VDD	
S_pad[20]	62	S[20]	IN
S_pad[19]	63	S[19]	IN
S_pad[18]	64	S[18]	IN
S_pad[17]	65	S[17]	IN
S_pad[16]	66	S[16]	IN
S_pad[15]	67	S[15]	IN
S_pad[14]	68	S[14]	IN
S_pad[13]	69	S[13]	IN
Freeze_pad	70	Freeze	IN

WEST

PAD NAME	PIN NUMBER	SIGNAL NAME	IN/OUT
cornergnd[0]	72	VSS	
S_pad[12]	73	S[12]	IN
S_pad[11]	74	S[11]	IN
S_pad[10]	75	S[10]	IN
S_pad[9]	76	S[9]	IN
S_pad[8]	77	S[8]	IN
S_pad[7]	78	S[7]	IN
S_pad[6]	79	S[6]	IN
S_pad[5]	80	S[5]	IN
S_pad[4]	81	S[4]	IN
S_pad[3]	82	S[3]	IN
S_pad[2]	83	S[2]	IN
S_pad[1]	84	S[1]	IN
S_pad[0]	85	S[0]	IN
Op_sel_pad[3]	86	S_eq_f_1	IN
Op_sel_pad[2]	87	S_eq_f_2	IN
Op_sel_pad[1]	88	R_eq_f_1	IN
Op_sel_pad[0]	89	R_eq_f_2	IN
R_pad[31]	90	R[31]	IN
R_pad[30]	91	R[30]	IN
R_pad[29]	92	R[29]	IN
R_pad[28]	93	R[28]	IN
R_pad[27]	94	R[27]	IN
R_pad[26]	95	R[26]	IN
R_pad[25]	96	R[25]	IN
R_pad[24]	97	R[24]	IN
R_pad[23]	98	R[23]	IN
R_pad[22]	99	R[22]	IN
R_pad[21]	100	R[21]	IN
R_pad[20]	101	R[20]	IN
R_pad[19]	102	R[19]	IN
R_pad[18]	103	R[18]	IN
R_pad[17]	104	R[17]	IN
R_pad[16]	105	R[16]	IN

SOUTH

PAD NAME	PIN NUMBER	SIGNAL NAME	IN/OUT
cornerpwr[1]	108	VDD	
R_pad[15]	109	R[15]	IN
R_pad[14]	110	R[14]	IN
R_pad[13]	111	R[13]	IN
R_pad[12]	112	R[12]	IN
R_pad[11]	113	R[11]	IN
coreground[1]	114	VSS	
R_pad[10]	115	R[10]	IN
R_pad[9]	116	R[9]	IN
R_pad[8]	117	R[8]	IN
R_pad[7]	118	R[7]	IN
R_pad[6]	119	R[6]	IN
R_pad[5]	120	R[5]	IN
R_pad[4]	121	R[4]	IN
R_pad[3]	122	R[3]	IN
R_pad[2]	123	R[2]	IN
R_pad[1]	124	R[1]	IN
R_pad[0]	125	R[0]	IN
coreground[0]	126	VSS	
clock_pad	127,128,129	VDD,VSS,Proc_clk	IN
Run_pad	130	Proc_run	IN
Zero_pad	131	Zero	OUT
Carry_pad	132	Carry	OUT
Ovfl_pad	133	ALU_error	OUT
F_enable_pad[1]	134	F_bus_en[1]	IN
F_enable_pad[0]	135	F_bus_en[0]	IN
reset_pad	136	ALU_reset	IN
ringpower[0]	137	VDD	
F1_pad[0]	138	F[0]	OUT
F1_pad[1]	139	F[1]	OUT
F1_pad[2]	140	F[2]	OUT
F1_pad[3]	141	F[3]	OUT
ringground[0]	142	VSS	
Flush_pad	143	Flush	IN

Table 7: Pin Assignments for the Chip

```
*******************************************************************************
                Genesil Screen Dump -- Thu Aug 18 13:54:42 1988
*******************************************************************************
nip: ~sfpu/sfpu/fpu                                            Timing Analyzer
-----------------------------Genesil Version v7.0------------------------------
IOLATION MODE
-------------------------------------------------------------------------------
Fabline: NSC_CN12A                       Corner: TYPICAL
 Junction Temperature:75 degree C        Voltage:5.00v
 External Clock: Proc_clk
Included setup files: default setup file
-------------------------------------------------------------------------------
                                  NO VIOLATIONS
 Hold time check margin: 2.0ns












-------------------------------------------------------------------------------
NSERT  MESSAGES  GRAPHICS  FORM          OVERLAY          RECORD      UTILITY
-------------------------------------------------------------------------------
BACK



-------------------------------------------------------------------------------


>TIMING>VIOLATIONS>
```

```
LABEL Don't let opcode setup affect clk
TEMP_VOLT 100 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Proc_clk
INPUT ALU_opcode[0] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[1] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[2] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[3] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[4] 0 1 -999.00 0.00 -999.00 0.00
INPUT R_eq_f_1 0 1 -999.00 0.00 -999.00 0.00
INPUT R_eq_f_2 0 1 -999.00 0.00 -999.00 0.00
INPUT S_eq_f_1 0 1 -999.00 0.00 -999.00 0.00
INPUT S_eq_f_2 0 1 -999.00 0.00 -999.00 0.00
INPUT Test 0 1 -999.00 0.00 -999.00 0.00
```

```
****************************************************************************
              Genesil Screen Dump -- Thu Aug 18 11:12:24 1988
****************************************************************************
hip: ~sfpu/sfpu/fpu                                          Timing Analyzer
-----------------------------Genesil Version v7.0-----------------------------
LOCK REPORT MODE
------------------------------------------------------------------------------
rabline: NSC_CN12A                        Corner: GUARANTEED
 Junction Temperature:100 deg C           Voltage:5.00v
 External Clock: Proc_clk
Included setup files:
 #0  ignore_setup          (Don't let opcode setup affect clk)
------------------------------------------------------------------------------
                              CLOCK TIMES (minimum)
Phase 1 High:    31.0   ns                Phase 2 High:      6.9   ns
              ----------                                ----------
Cycle (from Ph1):   148.5    ns           Cycle (from Ph2):   133.7    ns
                  ----------                                ----------
Minimum Cycle Time:   148.5    ns         Symmetric Cycle Time:   148.5    ns
                    ----------                                  ----------
------------------------------------------------------------------------------
                              CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    31.0    ns set by:
                              ----------
 ** Clock delay: 3.3ns (34.3-31.0)
  Node                             Cumulative Delay      Transition
  input/latch/(internal)                34.3                rise
  input/latch/n_freeze                  32.1                rise
  Freeze_pad/n_freeze                    8.5                rise
  Freeze_pad/n_freeze'                   4.9                rise
  Freeze                                 0.0                fall

Minimum Phase 2 high time is     6.9    ns set by:
                              ----------
 ** Clock delay: 2.9ns (9.7-6.9)
  Node                             Cumulative Delay      Transition
  output/flagreg/(internal)              9.7                fall
  output/flagreg/reset_2                 6.0                rise
  output/flagreg/reset_2'                5.9                rise
  output/flagreg/first                   4.7                fall
  output/flagreg/flush                   4.0                rise
  Flush_pad/flush                        2.6                rise
  Flush_pad/flush'                       2.0                rise
  Flush                                  0.0                rise

inimum cycle time (from Ph1) is  148.5     ns set by:
                                ----------
 ** Clock delay: 6.6ns (155.0-148.5)
  Node                             Cumulative Delay      Transition
  mult/multac/(internal)               155.0                rise
  mult/multac/mant_A[23]               112.5                fall
  input/a_high/mant_A[23]              107.8                fall
  input/a_high/mant_A[23]'             103.8                fall
  input/a_high/mant_Ax                 100.8                fall
  input/a_high/mant_Ax'                100.7                fall
```

```
  input/a_high/not_mant_Ax                 99.8          rise
  input/a_input/not_mant_Ax                99.2          rise
  input/a_input/not_mant_Ax'               96.8          rise
  input/a_input/INTER1_VAL1[29]            92.9          fall
  *input/a_input/(internal)                91.7          rise
  input/a_input/alu_out[29]                88.3          fall
  <ut/result_handler/alu_out[29]           81.0          fall
  <t/result_handler/alu_out[29]'           79.7          fall
  <put/result_handler/result[29]           76.4          fall
  output/expmux/result[5]                  76.4          fall
  output/expmux/exp_low[5]                 71.7          fall
  output/expmux/normexp[5]                 67.5          fall
  normalizer/exponent/normexp[6]           67.2          fall
  <rmalizer/exponent/normexp[6]'           66.9          fall
  <lizer/exponent/ADDSUB1_OUT[6]           65.8          fall
  normalizer/exponent/lead[1]              48.8          rise
  normalizer/cascade/lead[1]               48.7          rise
  normalizer/cascade/lead[1]'              43.9          rise
  normalizer/cascade/ao[1]                 42.8          fall
  normalizer/cascade/naza                  42.2          rise
  normalizer/cascade/aza                   41.1          fall
  normalizer/encodera/all_zero             41.0          fall
  normalizer/encodera/all_zero'            38.0          fall
  normalizer/encodera/s[7]                 36.8          fall
  normalizer/encodera/in[5]                34.6          rise
  adder/shift_mant/sum_mant[23]            34.2          rise
  adder/shift_mant/sum_mant[23]'           33.7          rise
  adder/shift_mant/addout[23]              30.8          rise
  <er/shift_mant/ADDSUB6_OUT[23]           29.5          rise
  adder/shift_mant/addsubsel                7.6          fall
  adder/sign_logic/addsubsel                7.6          fall
  adder/sign_logic/addsubsel'               6.3          fall
  adder/sign_logic/round_x                  4.8          fall
  adder/sign_logic/PHASE_A                  2.7          rise
  clock_pad/PHASE_A                         1.2          rise
  Proc_clk                                  0.0          rise

Minimum cycle time (from Ph2) is  133.7    ns set by:
                                 ----------
 ** Clock delay: 2.7ns (69.6-66.9) cycle_sharing disabled
  Node                              Cumulative Delay    Transition
  input/a_input/(internal)              150.9           rise
  input/a_input/alu_out[29]             147.4           fall
  <ut/result_handler/alu_out[29]        140.2           fall
  <t/result_handler/alu_out[29]'        138.8           fall
  <put/result_handler/result[29]        135.6           fall
  output/expmux/result[5]               135.6           fall
  output/expmux/exp_low[5]              130.9           fall
  output/expmux/normexp[5]              126.6           fall
  normalizer/exponent/normexp[6]        126.4           fall
  <rmalizer/exponent/normexp[6]'        126.1           fall
  <lizer/exponent/ADDSUB1_OUT[6]        125.0           fall
  normalizer/exponent/lead[1]           107.9           rise
  normalizer/cascade/lead[1]            107.9           rise
  normalizer/cascade/lead[1]'           103.0           rise
  normalizer/cascade/co[1]              102.3           fall
```

normalizer/cascade/co[1]'	102.2	fall
normalizer/cascade/nazc	101.1	rise
normalizer/cascade/azc	100.0	fall
normalizer/encoderc/all_zero	99.9	fall
normalizer/encoderc/all_zero'	98.6	fall
normalizer/encoderc/s[7]	97.3	fall
normalizer/encoderc/in[4]	95.0	rise
adder/shift_mant/sum_mant[6]	94.6	rise
adder/shift_mant/sum_mant[6]'	93.9	rise
adder/shift_mant/addout[6]	91.0	rise
<der/shift_mant/ADDSUB6_OUT[6]	89.7	rise
adder/shift_mant/postshift[0]	72.6	rise
adder/shift_mant/postshift[0]'	72.5	rise
<der/shift_mant/INTER4_VAL1[0]	70.7	rise
*adder/shift_mant/(internal)	69.1	fall
adder/shift_mant/c[0]	60.5	fall
adder/shift_logic/c[0]	60.5	fall
adder/shift_logic/c[0]'	59.8	fall
adder/shift_logic/sum2big	58.0	fall
adder/shift_logic/gt24	56.1	rise
adder/shift_logic/gt24'	56.0	rise
adder/shift_logic/or_out	54.7	fall
adder/shift_logic/exp_sum[0]	52.1	fall
adder/subtract/exp_sum[0]	52.1	fall
adder/subtract/exp_sum[0]'	51.9	fall
adder/subtract/subout[8]	48.7	rise
adder/subtract/subout[8]'	47.8	rise
adder/subtract/ADDSUB1_OUT[8]	46.4	rise
adder/subtract/b[7]	36.6	fall
input/b_high/b[7]	31.4	fall
input/b_high/b[7]'	13.5	fall
input/b_high/bexpsel[0]	10.0	rise
input/latch/bexpsel[0]	9.5	rise
input/latch/bexpsel[0]'	8.4	rise
input/latch/PHASE_B	3.7	rise
clock_pad/PHASE_B	2.4	rise
Proc_clk	0.0	fall

```
LABEL Reg. temp -- setup/hold/output
TEMP_VOLT 100 5.00
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Proc_clk
```

```
*****************************************************************************
                Genesil Screen Dump -- Thu Aug 18 11:00:59 1988
*****************************************************************************
hip: ~sfpu/sfpu/fpu                                            Timing Analyzer
------------------------------Genesil Version v7.0-----------------------------
ETUP AND HOLD MODE
------------------------------------------------------------------------------
abline: NSC_CN12A                          Corner: GUARANTEED
 Junction Temperature:100 deg C            Voltage:5.00v
 External Clock: Proc_clk
Included setup files:
 #0  include_setup          (Reg. temp -- setup/hold/output)
------------------------------------------------------------------------------
                        INPUT SETUP AND HOLD TIMES (ns)
```

nput	Setup Time Ph1(f)	Setup Time Ph2(f)	Hold Time Ph1(f)	Hold Time Ph2(f)	
LU_opcode[0]	---	19.0	---	-3.3	PATH
LU_opcode[1]	---	18.6	---	-3.2	PATH
ALU_opcode[2]	---	17.9	---	-2.3	PATH
LU_opcode[3]	---	17.8	---	-2.2	PATH
LU_opcode[4]	---	19.0	---	-3.5	PATH
LU_reset	---	4.4	---	-2.2	PATH
F_bus_en[0]	---	---	---	---	PATH
_bus_en[1]	---	---	---	---	PATH
lush	---	6.9	---	-0.8	PATH
Freeze	31.0	---	-13.8	---	PATH
roc_run	---	5.6	---	-3.9	PATH
[0]	---	3.9	---	-2.3	PATH
[10]	---	3.6	---	-2.0	PATH
R[11]	---	3.6	---	-2.0	PATH
[12]	---	3.5	---	-1.9	PATH
[13]	---	3.5	---	-1.9	PATH
R[14]	---	3.5	---	-1.9	PATH
[15]	---	3.5	---	-1.9	PATH
[16]	---	3.5	---	-1.9	PATH
[17]	---	3.5	---	-1.9	PATH
R[18]	---	3.6	---	-2.0	PATH
[19]	---	3.6	---	-1.9	PATH
[1]	---	3.8	---	-2.2	PATH
R[20]	---	3.5	---	-1.9	PATH
[21]	---	3.5	---	-1.9	PATH
[22]	---	3.4	---	-1.8	PATH
[23]	---	3.4	---	-1.8	PATH
R[24]	---	3.4	---	-1.8	PATH
[25]	---	3.5	---	-1.9	PATH
[26]	---	3.5	---	-1.9	PATH
R[27]	---	3.5	---	-1.9	PATH
[28]	---	3.5	---	-1.9	PATH
[29]	---	3.5	---	-1.9	PATH
[2]	---	3.8	---	-2.2	PATH
R[30]	---	3.5	---	-1.9	PATH
[31]	---	3.6	---	-1.9	PATH
[3]	---	3.8	---	-2.2	PATH
R[4]	---	3.8	---	-2.1	PATH
[5]	---	3.7	---	-2.1	PATH

[redacted]6]	---	3.7	---	-2.1	PATH
R[7]	---	3.7	---	-2.1	PATH
[redacted][8]	---	3.7	---	-2.0	PATH
[redacted]9]	---	3.6	---	-2.0	PATH
[redacted]_eq_f_1	---	9.3	---	-5.2	PATH
R_eq_f_2	---	9.7	---	-6.8	PATH
[redacted]0]	---	3.6	---	-1.9	PATH
[redacted]10]	---	3.3	---	-1.7	PATH
S[11]	---	3.3	---	-1.7	PATH
S[12]	---	3.3	---	-1.7	PATH
[redacted]13]	---	3.4	---	-1.8	PATH
[redacted]14]	---	3.4	---	-1.8	PATH
S[15]	---	3.4	---	-1.8	PATH
[redacted]16]	---	3.4	---	-1.8	PATH
[redacted]17]	---	3.4	---	-1.8	PATH
S[18]	---	3.5	---	-1.9	PATH
S[19]	---	3.5	---	-1.9	PATH
[redacted]1]	---	3.5	---	-1.9	PATH
[redacted]20]	---	3.5	---	-1.9	PATH
S[21]	---	3.6	---	-2.0	PATH
[redacted]22]	---	3.6	---	-2.0	PATH
[redacted]23]	---	3.6	---	-2.0	PATH
S[24]	---	3.6	---	-2.0	PATH
S[25]	---	3.7	---	-2.0	PATH
[redacted]26]	---	3.7	---	-2.1	PATH
[redacted]27]	---	3.7	---	-2.1	PATH
S[28]	---	3.8	---	-2.2	PATH
[redacted]29]	---	3.9	---	-2.2	PATH
[redacted]2]	---	3.4	---	-1.8	PATH
S[30]	---	3.9	---	-2.3	PATH
S[31]	---	3.9	---	-2.3	PATH
[redacted]3]	---	3.4	---	-1.7	PATH
[redacted]4]	---	3.3	---	-1.7	PATH
S[5]	---	3.3	---	-1.7	PATH
[redacted]6]	---	3.3	---	-1.7	PATH
[redacted]7]	---	3.3	---	-1.7	PATH
S[8]	---	3.3	---	-1.7	PATH
S[9]	---	3.4	---	-1.8	PATH
[redacted]eq_f_1	---	14.0	---	-8.8	PATH
[redacted]eq_f_2	---	14.4	---	-10.8	PATH
Test	---	3.3	---	-1.9	PATH

```
*****************************************************************************
            Genesil Screen Dump -- Thu Aug 18 11:01:59 1988
*****************************************************************************
hip: ~sfpu/sfpu/fpu                                          Timing Analyzer
-----------------------------Genesil Version v7.0-----------------------------
ritial Paths (setup/hold):
------------------------------------------------------------------------------
abline: NSC_CN12A                          Corner: GUARANTEED
 Junction Temperature:100 deg C            Voltage:5.00v
 External Clock: Proc_clk
ncluded setup files:
 #0  include_setup          (Reg. temp -- setup/hold/output)
------------------------------------------------------------------------------
hase 1, Setup time:    31.0ns (34.3-3.3)
  input/latch/(internal)                    34.3        rise
  input/latch/n_freeze                      32.1        rise
  Freeze_pad/n_freeze                        8.5        rise
  Freeze_pad/n_freeze'                       4.9        rise
  Freeze                                     0.0        fall

hase 1, Hold time:   -13.8ns (2.7-16.5)
  <code_logic/fplatch/(internal)            16.5        rise
  opcode_logic/fplatch/n_freeze             16.0        fall
  Freeze_pad/n_freeze                        5.4        fall
  Freeze_pad/n_freeze'                       2.5        fall
  Freeze                                     0.0        rise




------------------------------------------------------------------------------
```

```
*****************************************************************************
              Genesil Screen Dump -- Thu Aug 18 11:04:03 1988
*****************************************************************************
ip: ~sfpu/sfpu/fpu                                           Timing Analyzer
-----------------------------Genesil Version v7.0----------------------------
itial Paths (setup/hold):
-----------------------------------------------------------------------------
abline: NSC_CN12A                        Corner: GUARANTEED
 Junction Temperature:100 deg C          Voltage:5.00v
 External Clock: Proc_clk
ncluded setup files:
 #0  include_setup          (Reg. temp -- setup/hold/output)
-----------------------------------------------------------------------------

hase 2, Setup time:      9.7ns (14.4-4.7)
  input/a_input/(internal)                  14.4          rise
  input/a_input/op_sel[0]                    8.1          fall
  input/op_sel_logic/op_sel[0]               7.9          fall
  input/op_sel_logic/op_sel[0]'              6.2          fall
  input/op_sel_logic/r_eq_f_2                4.6          fall
  Op_sel_pad[0]/op_sel                       4.3          fall
  Op_sel_pad[0]/op_sel'                      3.7          fall
  R_eq_f_2                                   0.0          fall

ase 2, Hold time:     -6.8ns (4.7-11.5)
  input/a_input/(internal)                  11.5          rise
  input/a_input/op_sel[0]                    7.4          rise
  input/op_sel_logic/op_sel[0]               7.2          rise
  input/op_sel_logic/op_sel[0]'              5.8          rise
  input/op_sel_logic/r_eq_f_2                4.5          rise
  Op_sel_pad[0]/op_sel                       4.1          rise
  Op_sel_pad[0]/op_sel'                      3.8          rise
  R_eq_f_2                                   0.0          rise




-----------------------------------------------------------------------------
```

```
**************************************************************************************
                Genesil Screen Dump -- Thu Aug 18 11:05:57 1988
**************************************************************************************
hip: ~sfpu/sfpu/fpu                                              Timing Analyzer
------------------------------Genesil Version v7.0------------------------------
ritial Paths (setup/hold):
--------------------------------------------------------------------------------
abline: NSC_CN12A                          Corner: GUARANTEED
 Junction Temperature:100 deg C            Voltage:5.00v
 External Clock: Proc_clk
Included setup files:
 #0  include_setup           (Reg. temp -- setup/hold/output)
--------------------------------------------------------------------------------

hase 2, Setup time:    14.4ns (19.3-4.9)
   input/b_input/(internal)                       19.3          rise
   input/b_input/op_sel[2]                        13.0          fall
   input/op_sel_logic/op_sel[2]                   11.6          fall
   input/op_sel_logic/op_sel[2]'                   6.3          fall
   input/op_sel_logic/s_eq_f_2                     4.8          fall
   Op_sel_pad[2]/op_sel                            4.3          fall
   Op_sel_pad[2]/op_sel'                           3.7          fall
   S_eq_f_2                                        0.0          fall

hase 2, Hold time:   -10.8ns (4.8-15.6)
   input/b_input/(internal)                       15.6          rise
   input/b_input/op_sel[2]                        11.5          rise
   input/op_sel_logic/op_sel[2]                   10.2          rise
   input/op_sel_logic/op_sel[2]'                   5.9          rise
   input/op_sel_logic/s_eq_f_2                     4.6          rise
   Op_sel_pad[2]/op_sel                            4.2          rise
   Op_sel_pad[2]/op_sel'                           3.8          rise
   S_eq_f_2                                        0.0          rise



--------------------------------------------------------------------------------
```

```
******************************************************************************
              Genesil Screen Dump -- Thu Aug 18 11:06:16 1988
******************************************************************************
Chip: ~sfpu/sfpu/fpu                                         Timing Analyzer
----------------------------Genesil Version v7.0-----------------------------
OUTPUT DELAY MODE
------------------------------------------------------------------------------
Fabline: NSC_CN12A                        Corner: GUARANTEED
 Junction Temperature:100 deg C           Voltage:5.00v
 External Clock: Proc_clk
Included setup files:
 #0  include_setup          (Reg. temp -- setup/hold/output)
------------------------------------------------------------------------------
```

OUTPUT DELAYS (ns)

Output	Ph1(r) Delay Min	Max	Ph2(r) Delay Min	Max	Loading(pf)	
ALU_error	15.7	21.5	---	---	50.00	PATH
Carry	14.9	20.9	---	---	50.00	PATH
F[0]	20.1	27.8	21.9	27.8	50.00	PATH
F[10]	16.9	26.0	20.0	26.0	50.00	PATH
F[11]	16.9	26.0	20.0	26.0	50.00	PATH
F[12]	16.8	25.6	19.6	25.6	50.00	PATH
F[13]	16.8	25.6	19.6	25.6	50.00	PATH
F[14]	16.8	25.6	19.6	25.6	50.00	PATH
F[15]	16.6	25.6	19.6	25.6	50.00	PATH
F[16]	16.1	25.3	19.3	25.3	50.00	PATH
F[17]	16.1	25.3	19.3	25.3	50.00	PATH
F[18]	16.2	25.3	19.3	25.3	50.00	PATH
F[19]	16.3	25.3	19.3	25.3	50.00	PATH
F[1]	19.2	27.9	21.9	27.9	50.00	PATH
F[20]	16.3	25.5	19.6	25.5	50.00	PATH
F[21]	16.4	25.5	19.6	25.5	50.00	PATH
F[22]	16.4	25.5	19.5	25.5	50.00	PATH
F[23]	16.4	25.5	19.5	25.5	50.00	PATH
F[24]	16.6	25.3	19.4	25.3	50.00	PATH
F[25]	16.7	25.3	19.4	25.3	50.00	PATH
F[26]	16.7	25.4	19.4	25.4	50.00	PATH
F[27]	17.3	25.4	19.4	25.4	50.00	PATH
F[28]	14.4	23.3	16.9	23.3	50.00	PATH
F[29]	14.3	23.3	16.9	23.3	50.00	PATH
F[2]	19.7	27.9	21.9	27.9	50.00	PATH
F[30]	14.2	23.3	16.9	23.3	50.00	PATH
F[31]	15.0	23.3	16.8	23.3	50.00	PATH
F[3]	19.6	27.9	21.9	27.9	50.00	PATH
F[4]	19.3	26.4	20.5	26.4	50.00	PATH
F[5]	19.1	26.4	20.4	26.4	50.00	PATH
F[6]	19.0	26.4	20.4	26.4	50.00	PATH
F[7]	18.8	26.4	20.4	26.4	50.00	PATH
F[8]	16.9	26.0	20.0	26.0	50.00	PATH
F[9]	16.9	26.0	20.0	26.0	50.00	PATH
Zero	12.3	18.1	---	---	50.00	PATH

```
------------------------------------------------------------------------------
```

```
*******************************************************************************
           Genesil Screen Dump -- Thu Aug 18 11:06:55 1988

*******************************************************************************
hip: ~sfpu/sfpu/fpu                                           Timing Analyzer
------------------------------Genesil Version v7.0-------------+---------------
   Dest. Object       Connector         (Ph2)   Min      Max       BLOCK NAME
F enable pad[0] F bus en                    22.1     27.8        *CURRENT*
    F1 pad[0]       F                           22.1     27.8  PATHAlu_op_pad[0]
F enable pad[0] F bus en                    20.7     26.4          Alu_op_pad[1]
    F2 pad[0]       F                           20.7     26.4  PATHAlu_op_pad[2]
F enable pad[0] F bus en                    20.3     26.0          Alu_op_pad[3]
    F3 pad[0]       F                           20.3     26.0  PATHAlu_op_pad[4]
F enable pad[0] F bus en                    19.9     25.6          Carry_pad
    F4 pad[0]       F                           19.9     25.6  PATHF1_pad[0]
F enable pad[0] F bus en                    19.6     25.3          F1_pad[1]
    F5 pad[0]       F                           19.6     25.3  PATHF1_pad[2]
F enable pad[0] F bus en                    19.8     25.5          F1_pad[3]
    F6 pad[0]       F                           19.8     25.5  PATHF2_pad[0]
F enable pad[0] F bus en                    19.6     25.3          F2_pad[1]
    F7 pad[0]       F                           19.6     25.3  PATHF2_pad[2]
F enable pad[0] F bus en                    17.1     23.3          F2_pad[3]
    F8 pad[0]       F                           17.1     23.3  PATHF3_pad[0]
F enable pad[1] F bus en                    21.9     27.6          F3_pad[1]
    F1 pad[0]       F                           21.9     27.6  PATHF3_pad[2]
F enable pad[1] F bus en                    20.5     26.2          F3_pad[3]
    F2 pad[0]       F                           20.5     26.2  PATHF4_pad[0]
F enable pad[1] F bus en                    20.0     25.7          F4_pad[1]
    F3 pad[0]       F                           20.0     25.7  PATHF4_pad[2]
F enable pad[1] F bus en                    19.6     25.3          F4_pad[3]
    F4 pad[0]       F                           19.6     25.3  PATHF5_pad[0]
F enable pad[1] F bus en                    19.3     25.0          F5_pad[1]
    F5 pad[0]       F                           19.3     25.0  PATHF5_pad[2]
F enable pad[1] F bus en                    19.6     25.3          F5_pad[3]
    F6 pad[0]       F                           19.6     25.3  PATHF6_pad[0]
F enable pad[1] F bus en                    19.4     25.1          F6_pad[1]
    F7 pad[0]       F                           19.4     25.1  PATHF6_pad[2]
F enable pad[1] F bus en                    16.9     23.1          F6_pad[3]
    F8 pad[0]       F                           16.9     23.1  PATHF7_pad[0]
                                                                   F7_pad[1]
                                                                   * MORE *
---------------------------------------------------------------+--------------
```

```
***************************************************************************************
                Genesil Screen Dump -- Thu Aug 18 11:07:16 1988
***************************************************************************************
hip: ~sfpu/sfpu/fpu                                                     Timing Analyzer
----------------------------Genesil Version v7.0------------------------------------
IOLATION MODE
---------------------------------------------------------------------------------------
abline: NSC_CN12A                        Corner: GUARANTEED
 Junction Temperature:100 deg C          Voltage:5.00v
 External Clock: Proc_clk
Included setup files:
 #0  include_setup          (Reg. temp -- setup/hold/output)
---------------------------------------------------------------------------------------
                                  NO VIOLATIONS
 Hold time check margin: 2.0ns
---------------------------------------------------------------------------------------
```

```
LABEL High temp - no opcode setup - clk
TEMP_VOLT 150 4.50
HOLDTIME_MARGIN 2.00
SELECT_EXT_CLOCK Proc_clk
INPUT ALU_opcode[0] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[1] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[2] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[3] 0 1 -999.00 0.00 -999.00 0.00
INPUT ALU_opcode[4] 0 1 -999.00 0.00 -999.00 0.00
INPUT R_eq_f_1 0 1 -999.00 0.00 -999.00 0.00
INPUT R_eq_f_2 0 1 -999.00 0.00 -999.00 0.00
INPUT S_eq_f_1 0 1 -999.00 0.00 -999.00 0.00
INPUT S_eq_f_2 0 1 -999.00 0.00 -999.00 0.00
INPUT Test 0 1 -999.00 0.00 -999.00 0.00
```

```
*****************************************************************************
                Genesil Screen Dump -- Thu Aug 18 11:17:37 1988

*****************************************************************************
hip: ~sfpu/sfpu/fpu                                          Timing Analyzer
------------------------------Genesil Version v7.0-----------------------------
LOCK REPORT MODE
-----------------------------------------------------------------------------
abline: NSC_CN12A                          Corner: GUARANTEED
 Junction Temperature:150 deg C            Voltage:4.50v
 External Clock: Proc_clk
Included setup files:
 #0  ignore_high            (High temp - no opcode setup - clk)
-----------------------------------------------------------------------------
                             CLOCK TIMES (minimum)
hase 1 High:    34.7   ns                 Phase 2 High:     7.8   ns
               ----------                                 ----------
ycle (from Ph1):   166.0   ns             Cycle (from Ph2):   149.1   ns
                  ----------                                 ----------
Minimum Cycle Time:   166.0   ns          Symmetric Cycle Time:   166.0   ns
                     ----------                                  ----------
-----------------------------------------------------------------------------
                             CLOCK WORST CASE PATHS
Minimum Phase 1 high time is    34.7   ns set by:
                              ----------
 ** Clock delay: 3.5ns (38.1-34.7)
  Node                          Cumulative Delay      Transition
  input/latch/(internal)              38.1               rise
  input/latch/n_freeze                35.7               rise
  Freeze_pad/n_freeze                  9.5               rise
  Freeze_pad/n_freeze'                 5.5               rise
  Freeze                               0.0               fall

Minimum Phase 2 high time is     7.8   ns set by:
                              ----------
 ** Clock delay: 3.0ns (10.9-7.8)
  Node                          Cumulative Delay      Transition
  output/flagreg/(internal)           10.9               fall
  output/flagreg/reset_2               6.7               rise
  output/flagreg/reset_2'              6.6               rise
  output/flagreg/first                 5.2               fall
  output/flagreg/flush                 4.5               rise
  Flush_pad/flush                      2.9               rise
  Flush_pad/flush'                     2.3               rise
  Flush                                0.0               rise

nimum cycle time (from Ph1) is  166.0    ns set by:
                               ----------
 ** Clock delay: 7.1ns (173.1-166.0)
  Node                          Cumulative Delay      Transition
  mult/multac/(internal)             173.1               rise
  mult/multac/mant_A[23]             125.8               fall
  input/a_high/mant_A[23]            120.6               fall
  input/a_high/mant_A[23]'           116.2               fall
  input/a_high/mant_Ax               112.8               fall
  input/a_high/mant_Ax'              112.8               fall
```

```
  input/a_high/not_mant_Ax                111.8                 rise
  input/a_input/not_mant_Ax               111.1                 rise
  input/a_input/not_mant_Ax'              108.4                 rise
  input/a_input/INTER1_VAL1[29]           104.1                 fall
  *input/a_input/(internal)               102.8                 rise
  input/a_input/alu_out[29]                99.0                 fall
  <ut/result_handler/alu_out[29]           90.9                 fall
  <t/result_handler/alu_out[29]'           89.4                 fall
  <put/result_handler/result[29]           85.8                 fall
  output/expmux/result[5]                  85.8                 fall
  output/expmux/exp_low[5]                 80.5                 fall
  output/expmux/normexp[5]                 75.8                 fall
  normalizer/exponent/normexp[6]           75.5                 fall
  <rmalizer/exponent/normexp[6]'           75.2                 fall
  <lizer/exponent/ADDSUB1_OUT[6]           74.0                 fall
  normalizer/exponent/lead[1]              54.8                 rise
  normalizer/cascade/lead[1]               54.8                 rise
  normalizer/cascade/lead[1]'              49.4                 rise
  normalizer/cascade/ao[1]                 48.2                 fall
  normalizer/cascade/ao[1]'                48.1                 fall
  normalizer/cascade/naza                  47.5                 rise
  normalizer/cascade/aza                   46.3                 fall
  normalizer/encodera/all_zero             46.2                 fall
  normalizer/encodera/all_zero'            42.9                 fall
  normalizer/encodera/s[7]                 41.5                 fall
  normalizer/encodera/in[5]                39.0                 rise
  adder/shift_mant/sum_mant[23]            38.7                 rise
  adder/shift_mant/sum_mant[23]'           38.0                 rise
  adder/shift_mant/addout[23]              34.8                 rise
  <er/shift_mant/ADDSUB6_OUT[23]           33.4                 rise
  adder/shift_mant/addsubsel                8.4                 fall
  adder/sign_logic/addsubsel                8.4                 fall
  adder/sign_logic/addsubsel'               7.0                 fall
  adder/sign_logic/round_x                  5.2                 fall
  adder/sign_logic/PHASE_A                  2.9                 rise
  clock_pad/PHASE_A                         1.2                 rise
  Proc_clk                                  0.0                 rise

nimum cycle time (from Ph2) is  149.1    ns set by:
                                ----------
 ** Clock delay: 2.9ns (77.4-74.5) cycle_sharing disabled
  Node                            Cumulative Delay      Transition
  input/a_input/(internal)               168.0                 rise
  input/a_input/alu_out[29]              164.2                 fall
  <ut/result_handler/alu_out[29]         156.1                 fall
  <t/result_handler/alu_out[29]'         154.7                 fall
  <put/result_handler/result[29]         151.0                 fall
  output/expmux/result[5]                151.0                 fall
  output/expmux/exp_low[5]               145.8                 fall
  output/expmux/normexp[5]               141.1                 fall
  normalizer/exponent/normexp[6]         140.7                 fall
  <rmalizer/exponent/normexp[6]'         140.4                 fall
  <lizer/exponent/ADDSUB1_OUT[6]         139.2                 fall
  normalizer/exponent/lead[1]            120.1                 rise
  normalizer/cascade/lead[1]             120.0                 rise
  normalizer/cascade/lead[1]'            114.6                 rise
```

normalizer/cascade/co[1]	113.8	fall
normalizer/cascade/co[1]'	113.8	fall
normalizer/cascade/nazc	112.5	rise
normalizer/cascade/azc	111.3	fall
normalizer/encoderc/all_zero	111.2	fall
normalizer/encoderc/all_zero'	109.7	fall
normalizer/encoderc/s[7]	108.3	fall
normalizer/encoderc/in[4]	105.7	rise
adder/shift_mant/sum_mant[6]	105.3	rise
adder/shift_mant/sum_mant[6]'	104.5	rise
adder/shift_mant/addout[6]	101.3	rise
<der/shift_mant/ADDSUB6_OUT[6]	99.8	rise
adder/shift_mant/postshift[0]	80.8	rise
adder/shift_mant/postshift[0]'	80.6	rise
<der/shift_mant/INTER4_VAL1[0]	78.6	rise
*adder/shift_mant/(internal)	76.9	fall
adder/shift_mant/c[0]	67.2	fall
adder/shift_logic/c[0]	67.2	fall
adder/shift_logic/c[0]'	66.4	fall
adder/shift_logic/sum2big	64.3	fall
adder/shift_logic/gt24	62.2	rise
adder/shift_logic/gt24'	62.1	rise
adder/shift_logic/or_out	60.7	fall
adder/shift_logic/exp_sum[0]	57.8	fall
adder/subtract/exp_sum[0]	57.7	fall
adder/subtract/exp_sum[0]'	57.5	fall
adder/subtract/subout[8]	53.9	rise
adder/subtract/subout[8]'	53.0	rise
adder/subtract/ADDSUB1_OUT[8]	51.4	rise
adder/subtract/b[7]	40.5	fall
input/b_high/b[7]	34.7	fall
input/b_high/b[7]'	14.8	fall
input/b_high/bexpsel[0]	10.8	rise
input/latch/bexpsel[0]	10.3	rise
input/latch/bexpsel[0]'	9.1	rise
input/latch/PHASE_B	3.8	rise
clock_pad/PHASE_B	2.4	rise
Proc_clk	0.0	fall

```
ABEL High temp -- setup/hold/output
TEMP_VOLT 150 4.50
HOLDTIME_MARGIN 2.00
ELECT_EXT_CLOCK Proc_clk
```

```
*****************************************************************************
              Genesil Screen Dump -- Thu Aug 18 12:57:22 1988

*****************************************************************************
Chip: ~sfpu/sfpu/fpu                                          Timing Analyzer
------------------------------Genesil Version v7.0----------------------------
SETUP AND HOLD MODE
------------------------------------------------------------------------------
Fabline: NSC_CN12A                          Corner: GUARANTEED
  Junction Temperature:150 deg C            Voltage:4.50v
  External Clock: Proc_clk
Included setup files:
  #0  include_high          (High temp -- setup/hold/output)
------------------------------------------------------------------------------
```

INPUT SETUP AND HOLD TIMES (ns)

Input	Setup Time Ph1(f)	Setup Time Ph2(f)	Hold Time Ph1(f)	Hold Time Ph2(f)	
ALU_opcode[0]	---	21.3	---	-3.9	PATH
ALU_opcode[1]	---	20.8	---	-3.7	PATH
ALU_opcode[2]	---	20.1	---	-2.7	PATH
ALU_opcode[3]	---	20.0	---	-2.6	PATH
ALU_opcode[4]	---	21.3	---	-4.0	PATH
ALU_reset	---	5.0	---	-2.6	PATH
F_bus_en[0]	---	---	---	---	PATH
F_bus_en[1]	---	---	---	---	PATH
Flush	---	7.8	---	-1.1	PATH
Freeze	34.7	---	-15.4	---	PATH
Proc_run	---	6.4	---	-4.5	PATH
R[0]	---	4.4	---	-2.7	PATH
R[10]	---	4.1	---	-2.4	PATH
R[11]	---	4.1	---	-2.3	PATH
R[12]	---	4.1	---	-2.3	PATH
R[13]	---	4.0	---	-2.3	PATH
R[14]	---	4.0	---	-2.3	PATH
R[15]	---	4.0	---	-2.3	PATH
R[16]	---	4.0	---	-2.3	PATH
R[17]	---	4.0	---	-2.3	PATH
R[18]	---	4.1	---	-2.3	PATH
R[19]	---	4.1	---	-2.3	PATH
R[1]	---	4.4	---	-2.6	PATH
R[20]	---	4.1	---	-2.3	PATH
R[21]	---	4.0	---	-2.2	PATH
R[22]	---	3.9	---	-2.2	PATH
R[23]	---	4.0	---	-2.2	PATH
R[24]	---	4.0	---	-2.2	PATH
R[25]	---	4.0	---	-2.2	PATH
R[26]	---	4.0	---	-2.2	PATH
R[27]	---	4.0	---	-2.2	PATH
R[28]	---	4.0	---	-2.3	PATH
R[29]	---	4.0	---	-2.3	PATH
R[2]	---	4.4	---	-2.6	PATH
R[30]	---	4.1	---	-2.3	PATH
R[31]	---	4.1	---	-2.3	PATH
R[3]	---	4.3	---	-2.6	PATH
R[4]	---	4.3	---	-2.5	PATH
R[5]	---	4.3	---	-2.5	PATH

6]	---	4.2	---	-2.5	PATH
7]	---	4.2	---	-2.5	PATH
[8]	---	4.2	---	-2.4	PATH
9]	---	4.2	---	-2.4	PATH
eq_f_1	---	10.5	---	-5.9	PATH
eq_f_2	---	10.9	---	-7.8	PATH
0]	---	4.1	---	-2.3	PATH
10]	---	3.8	---	-2.1	PATH
11]	---	3.8	---	-2.1	PATH
[12]	---	3.9	---	-2.1	PATH
13]	---	3.9	---	-2.1	PATH
14]	---	3.9	---	-2.1	PATH
[15]	---	3.9	---	-2.2	PATH
16]	---	3.9	---	-2.2	PATH
17]	---	4.0	---	-2.2	PATH
18]	---	4.0	---	-2.2	PATH
[19]	---	4.0	---	-2.3	PATH
1]	---	4.0	---	-2.2	PATH
20]	---	4.1	---	-2.3	PATH
[21]	---	4.1	---	-2.4	PATH
22]	---	4.2	---	-2.4	PATH
23]	---	4.1	---	-2.4	PATH
24]	---	4.2	---	-2.4	PATH
[25]	---	4.2	---	-2.4	PATH
26]	---	4.2	---	-2.5	PATH
27]	---	4.3	---	-2.5	PATH
[28]	---	4.4	---	-2.6	PATH
29]	---	4.4	---	-2.7	PATH
2]	---	3.9	---	-2.1	PATH
30]	---	4.5	---	-2.7	PATH
[31]	---	4.5	---	-2.7	PATH
3]	---	3.9	---	-2.1	PATH
4]	---	3.8	---	-2.0	PATH
[5]	---	3.8	---	-2.0	PATH
6]	---	3.8	---	-2.0	PATH
7]	---	3.8	---	-2.0	PATH
8]	---	3.8	---	-2.0	PATH
[9]	---	3.9	---	-2.2	PATH
eq_f_1	---	15.7	---	-10.0	PATH
eq_f_2	---	16.2	---	-12.2	PATH
est	---	3.8	---	-2.2	PATH

****
Genesil Screen Dump -- Thu Aug 18 12:57:52 1988

****
hip: ~sfpu/sfpu/fpu Timing Analyzer

------------------------------Genesil Version v7.0------------------------------

UTPUT DELAY MODE

----

abline: NSC_CN12A Corner: GUARANTEED
Junction Temperature:150 deg C Voltage:4.50v
External Clock: Proc_clk
ncluded setup files:
#0 include_high (High temp -- setup/hold/output)

OUTPUT DELAYS (ns)

itput	Ph1(r) Delay Min	Max	Ph2(r) Delay Min	Max	Loading(pf)	
U_error	17.2	23.9	---	---	50.00	PATH
rry	16.5	23.1	---	---	50.00	PATH
[0]	22.1	30.9	24.3	30.9	50.00	PATH
[10]	18.6	28.8	22.2	28.8	50.00	PATH
11]	18.6	28.8	22.2	28.8	50.00	PATH
12]	18.5	28.4	21.8	28.4	50.00	PATH
F[13]	18.5	28.4	21.8	28.4	50.00	PATH
14]	18.5	28.4	21.8	28.4	50.00	PATH
15]	18.3	28.4	21.8	28.4	50.00	PATH
[16]	17.7	28.1	21.5	28.1	50.00	PATH
[17]	17.7	28.1	21.5	28.1	50.00	PATH
18]	17.9	28.1	21.4	28.1	50.00	PATH
19]	17.9	28.0	21.4	28.0	50.00	PATH
F[1]	21.1	30.9	24.3	30.9	50.00	PATH
20]	18.0	28.3	21.7	28.3	50.00	PATH
21]	18.0	28.3	21.7	28.3	50.00	PATH
[22]	18.1	28.3	21.7	28.3	50.00	PATH
[23]	18.1	28.3	21.7	28.3	50.00	PATH
24]	18.2	28.1	21.5	28.1	50.00	PATH
25]	18.3	28.1	21.5	28.1	50.00	PATH
[26]	18.4	28.1	21.5	28.1	50.00	PATH
27]	19.0	28.2	21.5	28.2	50.00	PATH
28]	15.8	25.9	18.7	25.9	50.00	PATH
[29]	15.7	25.9	18.7	25.9	50.00	PATH
[2]	21.7	30.9	24.3	30.9	50.00	PATH
30]	15.6	25.9	18.7	25.9	50.00	PATH
31]	16.5	25.9	18.7	25.9	50.00	PATH
[3]	21.6	31.0	24.3	31.0	50.00	PATH
4]	21.2	29.3	22.7	29.3	50.00	PATH
5]	21.1	29.3	22.7	29.3	50.00	PATH
[6]	20.9	29.3	22.7	29.3	50.00	PATH
[7]	20.7	29.3	22.7	29.3	50.00	PATH
8]	18.6	28.9	22.2	28.9	50.00	PATH
9]	18.6	28.9	22.2	28.9	50.00	PATH
ero	13.5	20.0	---	---	50.00	PATH

```
*****************************************************************************
              Genesil Screen Dump -- Thu Aug 18 12:57:06 1988
*****************************************************************************
hip: ~sfpu/sfpu/fpu                                         Timing Analyzer
------------------------------Genesil Version v7.0-------------+--------------
  Dest. Object      Connector        (Ph2)    Min      Max        BLOCK NAME
F enable pad[0] F bus en                  24.6     30.9         *CURRENT*
   F1 pad[0]        F                         24.6     30.9  PATHAlu_op_pad[0]
F enable pad[0] F bus en                  23.0     29.3         Alu_op_pad[1]
   F2 pad[0]        F                         23.0     29.3  PATHAlu_op_pad[2]
F enable pad[0] F bus en                  22.5     28.9         Alu_op_pad[3]
   F3 pad[0]        F                         22.5     28.9  PATHAlu_op_pad[4]
F enable pad[0] F bus en                  22.1     28.4         Carry_pad
   F4 pad[0]        F                         22.1     28.4  PATHF1_pad[0]
F enable pad[0] F bus en                  21.7     28.1         F1_pad[1]
   F5 pad[0]        F                         21.7     28.1  PATHF1_pad[2]
F enable pad[0] F bus en                  22.0     28.3         F1_pad[3]
   F6 pad[0]        F                         22.0     28.3  PATHF2_pad[0]
F enable pad[0] F bus en                  21.8     28.1         F2_pad[1]
   F7 pad[0]        F                         21.8     28.1  PATHF2_pad[2]
F enable pad[0] F bus en                  19.0     25.9         F2_pad[3]
   F8 pad[0]        F                         19.0     25.9  PATHF3_pad[0]
F enable pad[1] F bus en                  24.3     30.6         F3_pad[1]
   F1 pad[0]        F                         24.3     30.6  PATHF3_pad[2]
F enable pad[1] F bus en                  22.7     29.0         F3_pad[3]
   F2 pad[0]        F                         22.7     29.0  PATHF4_pad[0]
F enable pad[1] F bus en                  22.2     28.6         F4_pad[1]
   F3 pad[0]        F                         22.2     28.6  PATHF4_pad[2]
F enable pad[1] F bus en                  21.8     28.1         F4_pad[3]
   F4 pad[0]        F                         21.8     28.1  PATHF5_pad[0]
F enable pad[1] F bus en                  21.5     27.8         F5_pad[1]
   F5 pad[0]        F                         21.5     27.8  PATHF5_pad[2]
F enable pad[1] F bus en                  21.7     28.0         F5_pad[3]
   F6 pad[0]        F                         21.7     28.0  PATHF6_pad[0]
F enable pad[1] F bus en                  21.5     27.9         F6_pad[1]
   F7 pad[0]        F                         21.5     27.9  PATHF6_pad[2]
F enable pad[1] F bus en                  18.7     25.6         F6_pad[3]
   F8 pad[0]        F                         18.7     25.6  PATHF7_pad[0]
                                                                    F7_pad[1]
                                                                     * MORE *
---------------------------------------------------------------+--------------
```